REMARKS

Claims 1-21 are currently active.

The Examiner has found Claims 13-21 allowable, and Claims 4-12 objected to.

The Examiner has rejected Claims 1-3 as being unpatentable over Chiussi in view of Parruck and further in view of Newman and further in view of Yamanaka. Applicants respectfully traverse this rejection.

The Examiner, in the Office Action on page 2 beginning on line 14, states that the limitation of a parity stripe from which the packet is reconstructed with a parity stripe providing for error detection and correction can be found in figure 5, where the HCC stripe is meant to be the HEC or header error control as read in column 6, lines 14-23 and as seen in figure 5 "Old" packet and the "New" packet both contain the HEC parity stripe of Chiussi.

Applicants respectfully take strong difference to this statement by the Examiner in regard to Chiussi. Referring to column 6, lines 14-23, it simply states with reference to figure 5, we describe the format of the standard ATM cell 500 received at input ports 110 of figure 1. The ATM cell format includes a standard ATM header 501 which is 5 bytes long and a payload which is 40 bytes long. The ATM header has 4 bits of genetic flow control,

eight bits of virtual path identifier, 16 bits of virtual channel identifier 503, three bits of payload type indicator, one bit of cell loss priority, and 8 bits of header error control (HEC).

The header error control is simply a common error correction technique that is used when a signal is sent to be able to determine if there is an error in the signal. This has nothing to do with striping, or a parity stripe from which the packet can be reconstructed.

Moreover, just from the architecture of figure 1 of Chiussi and the fact that there is only one switch fabric, through which all the input ports are connected there is no striping or consideration for striping. This has been further clarified by the amendments to claim 1 which states the plurality of fabrics connected to the port cards for switching portions of the packet as stripes and a parity stripe from which the packet is reconstructed with a parity stripe providing for error detection and correction. This emphasizes the fact that a single packet is broken up into stripes. There is no teaching a suggestion in the applied art record of this limitation.

Additionally, in the Office Action, the Examiner states various reasons for the motivation of combining the references. Applicants respectfully traverse this conclusion. Patent law requires that the teachings to combine the references is found in the references themselves. There is always some reason that can be found to explain with hindsight why references can be combined. Efficiency is always a common reason to explain why references

can be combined to arrive at the claimed invention because by definition the presence of the claimed invention is generally more efficient than the various references in the applied art in regard to the claimed invention. However, that is not patent law. Furthermore, the architecture of a single switch fabric of Chiussi as opposed to a scheduler taught by Parruck for an ATM switch, or Newman which also has a completely different architecture are not combinable without significant redesign and development. Teachings from references cannot be taken out the context in which there found. This further supports the conclusion that the invention is not obvious from the applied art record. Accordingly, Claims 1-3 are not obvious over the applied art of record.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-21, now in this application be allowed.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

on 2/22/05

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